JPE 5-3-2

DSP Based Control of Interleaved Boost Converter

C. Sudhakarababu* and Mummadi Veerachary*†

*Dept. of Electrical Engineering, Indian Institute of Technology Delhi, New Delhi, India

ABSTRACT

In this paper a DSP based control scheme for the interleaved boost converter is presented. The mathematical model for the interleaved boost converter operating in a continuous inductor current mode is developed. A state-space averaging technique is used for modeling the converter system. A fixed frequency sliding mode controller is designed to ensure current distribution between the two converter modules and to achieve the load voltage regulation simultaneously. Necessary and sufficient conditions, using variable structure theory, are derived for the sliding mode to exist. The range of sliding mode controller coefficients is also determined. The designed controller capability, load distribution among the individual boost cells and load voltage regulation against source and load disturbances, are demonstrated through PSIM simulation results. A real-time controller based on ADMC401 DSP is developed. Experimental results are provided to validate the proposed control scheme.

Keywords: Digital control, Interleaved boost converter, Invariance condition, Ripple cancellation, Sliding-mode control.

1. Introduction

DC-DC converters are widely used in switch-mode power supplies. To meet increased demands, several new topologies are being developed that operate at a high efficiency rate and are relatively simple to control. In particular, buck topologies are finding wide applications whenever load voltage is less than the input source voltage. However, it has the disadvantage of the discontinuous input current increasing the ripple amplitude and electromagnetic interference (EMI). Boost topologies are suitable for universal input applications, provided load voltage always remains greater than the input voltage. It will also achieve a continuous input current, thereby reducing the input filtering requirements. However, even further reduction of the input ripple is required to enhance the performance of the converter system.

In recent years the demand for dc-dc converters has increased. Particularly, more attention is going towards development of compact power supplies having lightweight, more power density, high efficiency with faster dynamics etc. To meet increased demands several new topologies are introduced having higher efficiency and simple control. Power conversion through parallel-connected converters and load distribution among the converter modules[1-2] is one such area of interest. This parallel connected converter system has several advantages such as: (i) increases the system reliability, (ii) facilitates system maintenance, (iii) allows future expansions, (iv) low component stress devices can be used to achieve a cost effective design with reduction in system size and weight etc. Development of parallel converters with new control

Manuscript received, Jan. 22, 2005; revised April 11, 2005.
†Corresponding Author: mchary@ee.iitd.ernet.in, IIT, Delhi
Tel: +91-11-26596248, Fax: +91-11-26581606
*Dept. of Electrical Eng. Indian Institute of Technology Delhi

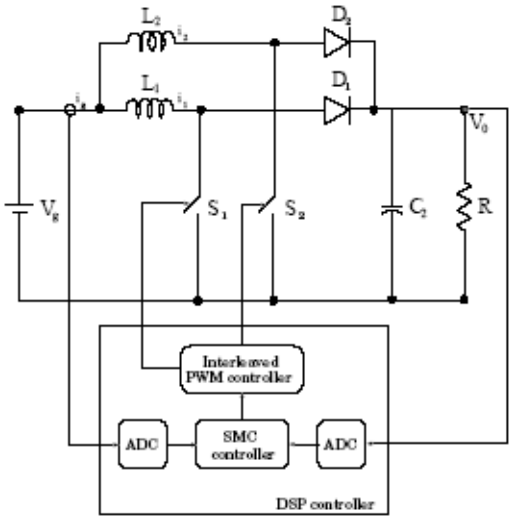

Fig. 1 DSP control of interleaved boost converter

strategies is being developed to increase the power processing capability and to improve the reliability of the power electronic system. In particular, dc-dc power conversion employing interleaved operation [3-6] has several advantages.

The advantages of constructing the power converters by means of interleaved parallel connected converters are: (i) ripple cancellation both in the input and output waveforms to maximum extent, and (ii) lower value of ripple amplitude, high ripple frequency in the resulting input and output waveforms. Furthermore, parallel connection of converters also reduces maintenance requirements, increases the reliability and fault tolerance, etc. During the past three decades, several aspects of dc-dc converters have been explored. These include modeling and analysis; improving both the steady-state and dynamic converter performance, etc. Among them, the control of high frequency dc-dc converters has attracted much research attention due to the inherent difficulties in achieving the desired characteristics, such as stiff line and load regulation, or robustness to uncertainties in the converter parameters [7-9]. Design of conventional controllers using a number of modules, parameter variations and large-signal disturbances is a difficult task. However, the fixed-frequency sliding mode control[10] technique in variable structure systems gives several advantages, in addition to flexibility in control-loop design, such as faster dynamics, good input voltage perturbation rejection, tight regulation of load voltage against line and load disturbances etc. So far, the analog control is predominant in power conversion closed-loop controllers due to its low implementation cost. However, analog control has several drawbacks such as a number of components and their susceptibility to aging and variation of environmental factors, which lead to degraded performance; the design is inflexible and its performance cannot be optimized for various operating conditions. The increasing performance and falling price of digital signal processors now provides the possibility of digital control with capability of adapting to the changes in converter dynamic characteristics.

Digital signal processors (DSP's) are finding wide application in many engineering fields and these are suitable in almost all high frequency power conversion applications. This is because of their ability to perform complex mathematical computations within minimum amount of time and efforts. Furthermore, the digital controller is flexible as the implementation involves only software instructions and is independent of the converter size. Implementing the sliding mode control, in conventional form, can be accomplished by using commercially available IC's and Op-amp circuits. However, these fixed-point analog controllers cannot adapt themselves to different operating conditions. To alleviate some of these disadvantages, a sliding mode controller realization in the digital domain for the interleaved boost converter, using Analog Devices DSP, is proposed in this paper. In this paper we design a simple fixed-frequency sliding mode controller for the interleaved boost converter as shown in Fig. 1. Firstly, the mathematical model of the converter is developed using a state-space domain[11] and then a sliding mode controller theory is derived in Section 2. Section 3 discusses the digital implementation of the sliding mode controller. Simulation and real-time implementation results are discussed and compared in Section 4. Conclusions follow in the final section.

2. State-space modeling of the interleaved boost converter

In this paper we design a sliding mode controller for the interleaved boost converter as shown in Fig. 1. It has been proved in the literature that the sliding mode controller is more robust against converter parameter uncertainties and

external disturbances, etc. In this instance, the sliding mode controller is designed to achieve the load voltage regulation against the line and load disturbances. To find the sliding regime which exists for this system we need to develop, firstly, a converter model. It is then required to find the range of sliding coefficients, necessary and sufficient conditions, etc. To develop the sliding mode theory for the two-cell interleaved converter system we start with the assumption that each boost cell inductor current is continuous. With this assumption we now develop the model for the converter in the state-space domain given below. For the two-cell interleaved boost converter the phase difference of 180^0 between two converter switching signals will result in minimum ripples both on the source and load sides. For these assumed switching signals more topologies and operating modes are possible depending on the switching frequency, load and duty ratio. In this analysis we will be discussing the continuous inductor current mode of operation. Even in the continuous inductor current mode of operation two cases will arise: (i) duty ratio D<50%, (ii) D>50%. In any of the above cases four modes of operation results in one input cycle of operation. In the following lines mathematical model for the interleaved boost converter is developed for the duty ratio D<50 % case. In this case there are four switching states for the converter, Mode-1: $0<t\le d_1T$ the devices S_1, D_2 are conducting; Mode-2: $d_1T<t\le(d_1+d_2)T$ the the devices D_2, D_1 are conducting; Mode-3: $(d_1+d_2)T<t\le(d_1+d_2+d_3)T$ the devices S_2, D_1 are conducting; Mode-4: $(d_1+d_2+d_3)T<t<(d_1+d_2+d_3+d_4)T$ the devices D_1, D_2 are conducting, and the corresponding circuits can easily be drawn. The equations for these four different circuits are developed, detailed equations are not given here, and the corresponding state models are obtained given in the following lines.

Mode-1:

$$\dot{X}_1 = [A_1][X] + [B_1]U \quad (1)$$

Mode-2:

$$\dot{X}_2 = [A_2][X] + [B_2]U \quad (2)$$

Mode-3:

$$\dot{X}_3 = [A_3][X] + [B_3]U \quad (3)$$

Mode-4:

$$\dot{X}_4 = [A_4][X] + [B_4]U \quad (4)$$

where $[A_i]$ and $[B_i]$, i=1,2,3,4 matrices are given by

$$A_1 = \begin{bmatrix} -\frac{r_1}{L_1} & 0 & 0 \\ 0 & -\frac{r_2}{L_2} & -\frac{1}{L_2} \\ 0 & \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}; \quad B_1 = \begin{bmatrix} \frac{1}{L_1} & 0 \\ \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C} \end{bmatrix}$$

$$A_2 = \begin{bmatrix} -\frac{r_1}{L_1} & 0 & -\frac{1}{L_1} \\ 0 & -\frac{r_2}{L_2} & -\frac{1}{L_2} \\ \frac{1}{C} & \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}; \quad B_2 = \begin{bmatrix} \frac{1}{L_1} & 0 \\ \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C} \end{bmatrix}$$

$$A_3 = \begin{bmatrix} -\frac{r_1}{L_1} & 0 & -\frac{1}{L_1} \\ 0 & -\frac{r_2}{L_2} & 0 \\ \frac{1}{C} & 0 & -\frac{1}{RC} \end{bmatrix}; \quad B_3 = \begin{bmatrix} \frac{1}{L_1} & 0 \\ \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C} \end{bmatrix}$$

$$A_4 = \begin{bmatrix} -\frac{r_1}{L_1} & 0 & -\frac{1}{L_1} \\ 0 & -\frac{r_2}{L_2} & -\frac{1}{L_2} \\ \frac{1}{C} & \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}; \quad B_4 = \begin{bmatrix} \frac{1}{L_1} & 0 \\ \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C} \end{bmatrix}$$

Taking the average of the above four state models results in the following average state-space model when there is no load disturbance, $i_L=0$.

$$\dot{X} = [A][X] + [B]U \quad (5)$$

where $(d_1+d_2+d_3+d_4)=1$, $[A]=(A_1d_1+A_2d_2+A_3d_3+A_4d_4)$, $[B]=(B_1d_1+B_2d_2+B_3d_3+B_4d_4)$. The corresponding [A] and [B] matrices are

$$A = \begin{bmatrix} -\frac{r_1}{L_1} & 0 & -\frac{(d_2+d_3+d_4)}{L_4} \\ 0 & -\frac{r_2}{L_2} & -\frac{(d_1+d_2+d_4)}{L_2} \\ \frac{(d_2+d_3+d_4)}{C} & \frac{(d_1+d_2+d_4)}{C} & -\frac{1}{RC} \end{bmatrix};$$

$$B = \begin{bmatrix} \frac{1}{L_1} & 0 \\ \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C} \end{bmatrix}; \quad [X] = \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_0 \end{bmatrix}; \quad [U] = \begin{bmatrix} V_g \\ 0 \end{bmatrix}$$

On the similar lines given above the state-space model for the D>50% case can also be obtained. Due to space constraints detailed modeling equations are not given here. However, the final state-space average model is given below for ready reference.

$$A = \begin{bmatrix} -\frac{r_1}{L_1} & 0 & -\frac{d_4}{L_1} \\ 0 & -\frac{r_2}{L_2} & -\frac{d_2}{L_2} \\ \frac{d_4}{C} & \frac{d_2}{C} & -\frac{1}{RC} \end{bmatrix}; \quad B = \begin{bmatrix} \frac{1}{L_1} & 0 \\ \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C} \end{bmatrix}$$

We consider the sliding surface as a combination of load voltage and input current given below.

$$S = k_1 i_g + k_2 \int \left(V_{ref} - v_0\right) d\tau + k_3 \left(V_{ref} - v_0\right) \quad (6)$$

where $i_g=(i_1+i_2)$. In case of sliding motion over the intersection of the switching surface, the invariance condition $S = \dot{S} = 0$ is satisfied. Applying the above invariance condition results in the following equation:

$$k_1 \frac{di_g}{dt} - k_2 \left(V_{ref} - v_0\right) - k_3 \frac{dv_0}{dt} = 0 \quad (7)$$

Substituting for (dv_0/dt), (di_g/dt) in the above equation from the state-model, 5, results in the following expression;

$$u_{eq} = \frac{\left[N_1 - \left(\frac{k_1 k_3 L i_g}{C}\right) - r k_1 i_g + N_2 - k_1 V_g\right]}{\left(v_0 - \frac{k_3 L i_g}{C}\right)} \quad (8)$$

$$N_1 = v_0 \left(1 + \frac{k_3 L}{RC}\right); \quad N_2 = k_2 L \left(V_{ref} - v_0\right)$$

Since the equivalent control is bounded $(0<u_{eq}<1)$ then the above equation becomes

$$0 < \left[N_1 + \frac{k_3 v_0 L}{RC}\right] < V_g \quad (9)$$

where 'k_1=1' and 'r' neglected since 'r<<R'. To get the constraint on the coefficient 'k_3' we substitute the condition for equilibrium point '$V_{ref}=v_0$' and for the interleaved boost converter '$V_{ref}\geq V_g$' then the above in-equality becomes

$$0 < k_3 < \frac{RCV_g}{LV_{ref}}$$

or

$$0 < \frac{k_3 L V_{ref}}{RC} < V_g \quad (10)$$

To get the range of values for the 'k_2' we will substitute eqn. 10 in eqn. 9 and after simplification results the following in-equality

$$0 < \left[N_2 + \frac{k_3 L v_0}{RC}\right] < \left[\frac{k_3 L V_{ref}}{RC} + \left(V_{ref} - v_0\right)\right] \quad (11)$$

simplifying further

$$0 < N_2 < \left[\frac{k_3 L V_{ref}}{RC} - \frac{k_3 L v_0}{RC} + \left(V_{ref} - v_0\right)\right]$$

or

$$0 < k_2 < \left[1 + \frac{k_3 L}{RC}\right] \quad (12)$$

3. Digital implementation of sliding mode controller

The proposed sliding mode controller algorithm, for the interleaved boost converter, is implemented using the Analog Devices ADMC401 DSP EVM module [12]. This ADMC401 module has the following major features: (i) fixed point 16-bit processor with 76.92 ns at 13 MHz clock frequency, (ii) 16-bit arithmetic and logic unit with 26 MIPS performance, (iii) three independent PWM generation units, (iv) 8 independent 12-bit ADC channels with simultaneous sampling and less than 2 μs for conversion of all channels, (iv) independent 12-bit serial DAC channel. The instantaneous load voltage and voltage proportional to the inductor current are sensed by the LEM LV25-P voltage sensor, ABB EL50P1BB current sensor, respectively. These voltage and current sensor outputs are given to the two independent ADC channels of ADMC401 module. The switching frequency of the converter and

sampling frequency of ADC is 100 kHz. Though the sliding surface given by eqn. 6 appears to be simple, it has to be represented in a form that can be easily implemented in the digital domain. In the following lines we will present the necessary steps involved in digitization [12] of the sliding mode controller. To start with we will again consider the sliding surface equation.

$$S = S_i + S_v \tag{13}$$

where $S_i = k_1 i_g$, $S_v = k_2 \int (V_{ref} - v_0) d\tau + k_3 (V_{ref} - v_0)$

In the discretization process, firstly, we will convert the control function 'S_v', the continuous time signal, into discrete form.

$$S_v = \left[\frac{k_2}{s} + k_3 \right] (V_{ref} - v_0) \tag{14}$$

$$S_v = k_3 \left[\frac{k_2}{k_3 s} + 1 \right] (V_{ref} - v_0) \tag{15}$$

The above mentioned equation needs to be converted into a discrete time domain, which involves replacing the integral operation by the discrete summation. Although several methods are available for this conversion, we have used an improved first order hold approach, where-in trapezoidal areas are used in discrete summation. The method is described in the following lines. In the zero order hold case the integral operation is approximated by accumulating the rectangular areas and involves a time lag of T/2. In the case of first order hold summation of the trapezoidal areas, results will give the integral operation. Let the sum of the trapezoidal areas up to the k^{th} sample equal S_k then, the integration up to the next sample time, (k+1), is obtained as

$$S_{(k+1)} = S_k + \frac{(H_k + H_{(k+1)}) T_{samp}}{2} \tag{16}$$

where 'T_{samp}' is the sampling time; H_k, '$H_{(k+1)}$' are the signal values at k^{th}, $(k+1)^{th}$ sampling instants, respectively. The above equation is now represented in z-domain as

$$zS_s = S_z + \frac{(z+1) H_z T_{samp}}{2} \tag{17}$$

Simplification results in the following equation

$$S_s = \frac{(z+1) H_z T_{samp}}{2(z-1)} \tag{18}$$

The above equation gives the z-domain equivalent of continuous time integration, 1/s. Therefore, the eqn. 14 in z-domain becomes

$$S_v(z) = k_3 \left[k_{23} \frac{(z+1) H(z) T_{samp}}{2(z-1)} + 1 \right] E(z) \tag{19}$$

where $k_{23}=k_2/k_3$, $E(z)=(V_{ref}(z)-v_0(z))$. On simplification the above equation becomes

$$(z-1) S_v(z) = k_3 [(a+1)z + (a-1)] E(z) \tag{20}$$

where $a = \frac{k_{23} T_{samp}}{2}$, The above equation represents the following difference equation.

$$S_v(k+1) = k_3 [(a+1) E_{(k+1)} + (a-1) E_k] + S_v(k) \tag{21}$$

Substituting the above equation in eqn. 13 results into the final sliding surface in discrete form and it is given below.

$$S_v'(k+1) = k_1 i_g(k) + S_v(k+1) \tag{22}$$

The above control law is a simple equation consisting of only multiplication and accumulates in operation and can easily be implemented in the digital domain. However, in ADMC401 the data is represented in 16-bit fixed-point notation, which requires all the coefficients and signal levels to be brought into 1.15 format. This can be achieved by introducing a common scaling factor for the above equation such that all the coefficients lie in the range of -1 and 1. Further, the de-scaling becomes easier, simple right shifting operation, if the scaling factor is chosen as a power of 2. Multiplying scaling factor 'N_0' on either sides of the above equation results

$$N_0 S_v(k+1) = N_1 [i_{L1}(k) + E(k)] + N_2 E(k+1) + N_0 S_v(k) \tag{23}$$

where $N_L=N_0.k_1$; $N_2=k_3 N_0(a+1)$; $N_1=k_3 N_0(a-1)$. At times, in the process of controller loop implementation it so happens that '$N_0 S_v(k+1)$' exceeds the limit of -1 and 1. This is mainly due to wind-up of the integral part. Such problems can easily be handled by putting a saturation limit

on the '$N_0S_v(k+1)$'. In order to increase the accuracy of controller implementation, particularly when we use 16 bit representation and taking repeated summation on small increments the present summation may not be significantly different from the preceding summation value. In such cases, it is possible with the ADMC401, by using auxiliary registers to handle the data processing in 32-bit format and finally converting the end results into 16-bit form, which we can use in the subsequent calculations. We have successfully implemented the controller, discussed above, in the Analog Devices ADMC401 DSP EV module. The controller algorithm is given in the flowchart, shown in Fig. 2. In the present analysis we have computed the parameters of the discrete controller which are tabulated in Table 1.

Table 1 Discrete controller parameter values

T_{samp}	10 μs
N_L	0.05
N_0	1.0
N_1	-0.57
N_2	0.63

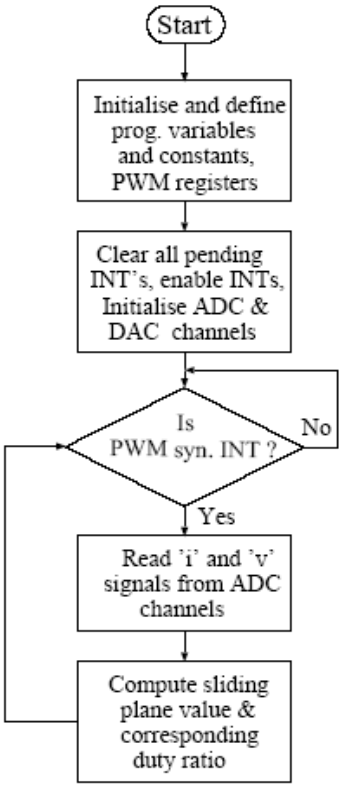

Fig. 2 DSP program flow chart

4. Results and discussions

Comprehensive simulation studies were made to verify the designed sliding mode controller for the interleaved boost converter. To verify the theoretical analysis, developed in the preceding Sections, the following design example was considered. A 100 W interleaved boost converter was constructed for this investigation. The converter parameters chosen for these studies are: r_1=40 Ω, r_2=43 Ω, r_c=1.05 Ω, L_1=125.6 μH, L_2=123.7 μH, C=9.2 μF, R=25 Ω. The converter and sliding mode controller are developed in the PSIM simulator environment. For the converter parameters, mentioned above, the range of sliding mode coefficients, k_1, k_2 and k_3, are computed from the equations given in Section 2. These coefficients for a reference voltage of 'V_{ref}=50 V' work out to be k_1=1, ($0<k_2<12294$), ($0<k_3<0.922$). To analyze the converter regulation performance, several large-signal simulations studies have been made for different operating conditions and sliding coefficients were tuned for optimum response. These simulation results reveal that the designed sliding mode controller is capable of regulating the load voltages against line and load disturbances. For illustration of load voltage regulation, against supply voltage and load disturbances, large-signal responses for one particular operating condition are given here: (i) load resistance change from 25 →19 Ω, (ii) supply voltage change from 30 → 23 V, and these results are given in Figs. 3 and 4, respectively. However, due to the presence of the closed loop sliding mode controller the load voltage is undergoing dynamics and settling to reference set point, V_{ref}=50 V, within a relatively small amount of time. Simulation results indicate that during the initial start-up period the currents and voltage are undergoing oscillations. This is mainly due to the effect of built-in integration methods available in the PSIM simulator [13]. The enlarged steady-state simulation results are shown in Fig. 5. For verification of simulation analysis results the experimental results were given in the following lines.

To verify the proposed controlling method of interleaved boost converter an experimental prototype control circuit with parameter values mentioned above has been built and measurements were taken from the prototype. The semiconductor devices used are an International

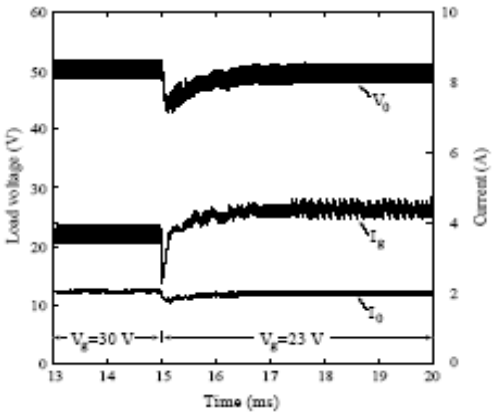

Fig. 3 Dynamic response of load voltage and current

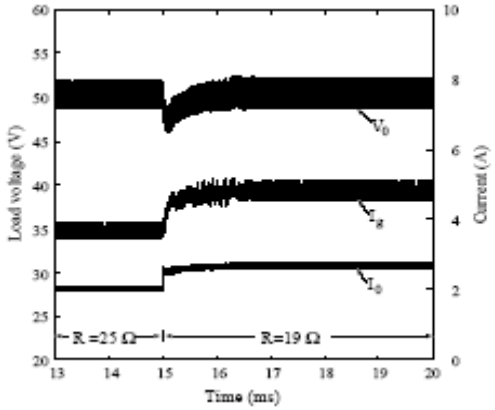

Fig. 4 Dynamic response of load voltage and current

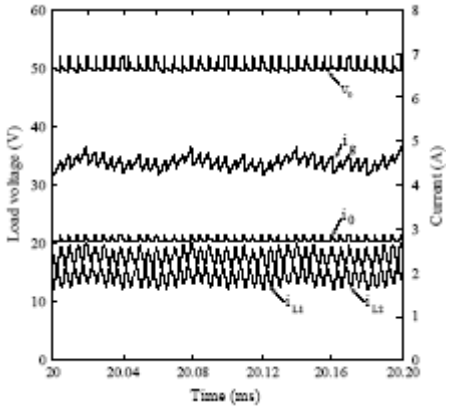

Fig. 5 Enlarged steady-state waveforms

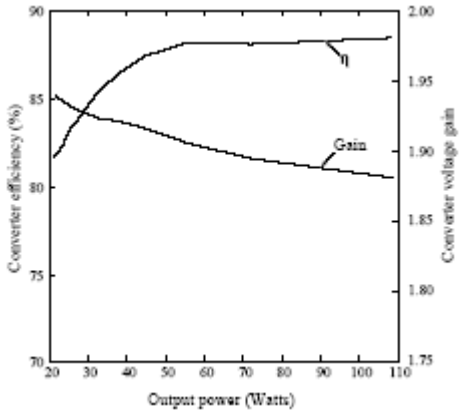

Fig. 6 Experimental efficiency and voltage gain variation with load power

Rectifier IRF530 power MOSFET, and a Motorola MUR820 fast recovery diode. The inductors are made of a toroidal core, TDK: HF70 T, whose dimensions are 100X12X7 mm. The switching device, MOSFET, is driven by an international rectifier IR2110 gate driver. IC 6N137 is used for isolation purposes. The converter parameters are the same as those used in simulation studies. Buffer circuits are used in between the power converter sensors, voltage and current sensors, and the DSP for safe operation of the ADC channels.

Initially, the steady-state performance of the interleaved boost converter is measured for different input voltages, load values and duty ratios. However, few performance measurements were given here for verification. For one particular duty ratio, 0.5, and input voltage, 25 V, the steady-state voltage gain variation and efficiency variation with load power is measured. The results are plotted in Fig. 6. These measurements indicate that the voltage gain of the converter is decreasing with increasing values of load power. This is mainly due to the voltage drop occurring in the non-idealities of the converter. Theoretically at duty ratio of 0.5 the converter should give almost twice the input voltage. In this case input voltage is 25 V and load voltage obtained at a load of 100 W is 47.03 V. The difference of 3 V is dropping down in the converter parasitic elements. The measured efficiency variation of the converter, for different loads is also plotted in the same figure.

The sliding mode controller is implemented using an Analog device ADMC401 DSP EVM module. The inputs to the DSP are the analog load voltage and voltage proportional to inductor current signals, within the range of ±2.0 V (4 V peak-to-peak), which are given to the independent ADC channels available on the ADMC processor board.

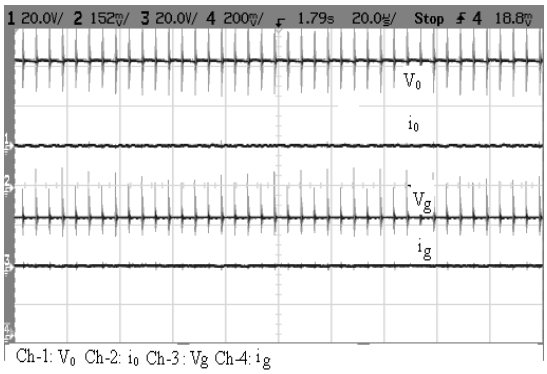

Fig. 7 Converter steady-state waveforms of interleaved boost converter

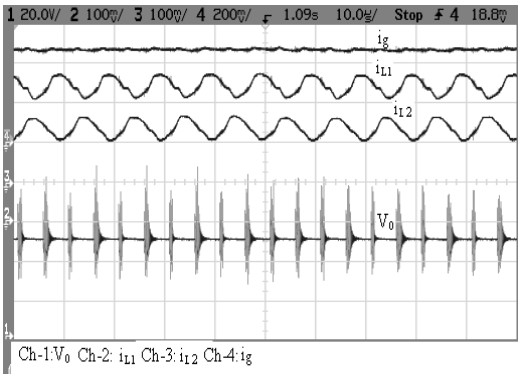

Fig. 10 Enlarged waveforms under closed loop control conditions at 100 kHz

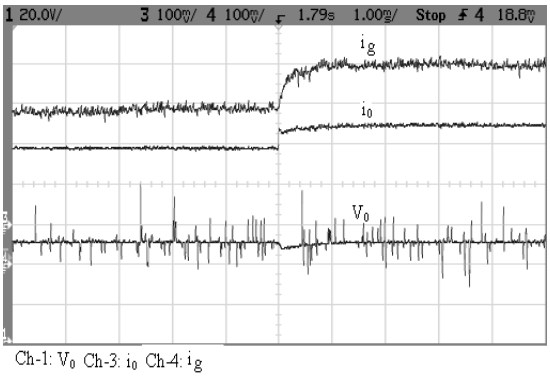

Fig. 8 Dynamic response of load voltage, current and source current at 100 kHz (load disturbance)

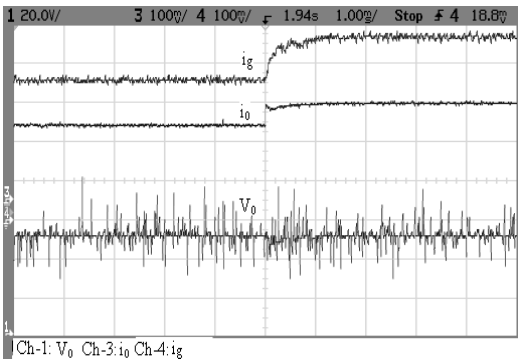

Fig. 11 Dynamic response of load voltage, current and source current at 150 kHz (load disturbance)

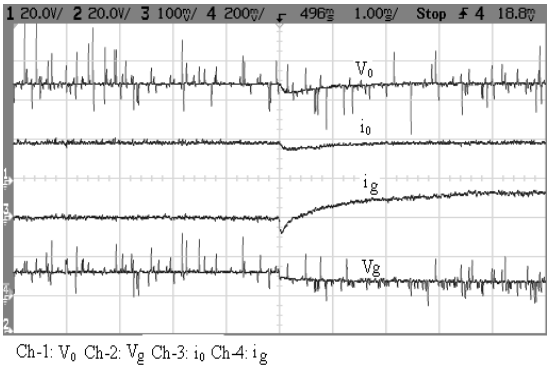

Fig. 9 Dynamic response of load voltage, current and source current at 100 kHz (source disturbance).

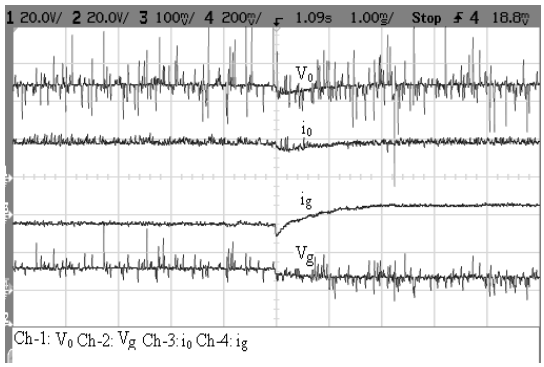

Fig. 12 Dynamic response of load voltage, current and source current at 150 kHz (source disturbance).

The controller algorithm processes these sampled voltage and current signals and sends out a PWM signal of appropriate duty ratio over the programmed PWM channels.

These channels are connected to the MOSFET drivers through an isolating opto-coupler. The experimental converter steady-state waveforms were measured and these are shown in Fig. 7. The experimental observations of

large-signal responses against source and load disturbances are taken for an operating frequency of 100 kHz: (i) load resistance change from 25 → 19 Ω, (ii) supply voltage change from 30 → 23 V, and these results are given in Figs. 8 and 9. These results indicate that the load voltage is remaining constant at the reference voltage of 50 V with a small amount of superimposed ripple. These observations, Figs. 8 and 9 are in close agreement with those obtained from simulation results shown in Fig. 3 and 4. For illustration of closed loop steady-state performance, the waveforms are recorded for one operating condition and these are shown in Fig. 10. To demonstrate the controller effectiveness a set of experimental results, for the identical conditions as mentioned above, were measured for the operating frequency of 150 kHz and these are shown in Figs. 11 and 12. Comparing these dynamic responses, obtained at 150 kHz, with Figs. 8 and 9 reveals that slight improvement in the dynamic response time. However, increasing the switching frequency increases switching ripple in the load voltage.

The experimental results closely match with those obtained from the simulated results. However, slight discrepancies in the experimental and simulation results are mainly due to the voltage drops in the parasitic components. In simulation the input supply voltage is stiff even if the load is increased. However, in an experimental system the source voltage slightly decreases with an increase in load. Due to this fact simulation results are slightly different form the experimental values. Furthermore, the analysis was made on the assumption that all the switching devices are ideal, i.e. in the modeling, non-idealities of the converter such as forward voltage drops, on-state resistances of the switching devices and other parasitic components are not taken into account. In simulation the step disturbance created is instantaneous while in the experimentation the step disturbances were created manually which may not be considered sudden step as that created in the simulation profile. Another important point is that, while developing simulators, developers normally provide their own equation solvers, which mainly restricts the step size for a given problem during simulation. Because of these facts the experimental dynamic responses were slightly different from simulated responses.

5. Conclusions

A mathematical model for the interleaved boost converter operating in continuous current mode was developed first and then a fixed frequency sliding mode controller was designed to achieve load voltage regulation. Necessary and sufficient conditions have been deduced using variable structure theories. Effectiveness of the proposed sliding mode controller for the interleaved boost converter was demonstrated using PSIM simulations. Detailed implementation of the discrete sliding mode controller using ADMC401 was discussed and implemented in real-time for different switching frequencies. These results demonstrate that the dynamic response can be improved slightly by increasing the switching frequency. However, we can't implement very high switching frequencies, which are mainly restricted by the sampling frequency of the ADC's and maximum operating frequencies of the switching devices.

References

[1] B. Choi, B. H. Cho, R. B. Ridley, F. C. Lee, “Control strategy for multi-module parallel converter system," IEEE Proc. on Power Electronic Specialists Conference, 1990, pp. 225-234.

[2] K. Siri, C. Q. Lee, “Current distribution control for parallel connected converters," IEEE Trans. on Aerospace and Electronic Systems, 1992, Vol. 28(3), pp. 829-840.

[3] David J. Perreault, John G. Kassakian, “Distributed interleaving of paralleled power converters," IEEE Trans. on Power Electronics, Vol. 9(4), pp. 405-413, 1994.

[4] Roberto Giral, Luis Martinez-Salamero, Sigmond Singer, “Interleaved converters operation based on CMC," IEEE Trans. on Power Electronics, Vol. 14(4), pp. 643-652, 1999.

[5] Veerachary. M, Senjyu. T, Uezato. K, “Modeling and analysis of interleaved dual boost converter,” IEEE International Symposium on Industrial Electronics (ISIE), Vol. 2, pp. 718 – 722, 2001.

[6] Xudong Huang, Xiaoyan Wang, Jeremy Ferrell, Xingyi Xu, Lizhi Zhu, “Parasitic ringing and design issues of high power interleaved boost converters," IEEE Proc. on Power Electronics Specialist Conference, 2002, pp. 30-35.

[7] H. Sira Ramirez, "Sliding motions in bilinear switched networks," IEEE Trans. On Circuits and Systems, 1987, Vol. 34, pp. 919-933.

[8] R. Venkataraman, A. Sabanovic, S. Cuk, "Sliding mode

control of dc-dc converters," IEEE Proc. on IECON, 1985, pp. 251-258.
[9] Marioano Lopez, Luis Garcia, Miguel Castilla, Oscar Lopez, “Control loop design using sliding mode and linear control techniques," IEEE conference APEC'00, pp. 390-394.
[10] Sonia Ferreira Pinto, J. Fernando A. Silva, "Constant frequency sliding-mode and PI linear controllers for power rectifiers: A comparison," IEEE Trans. On Ind. Electronics, 1999, Vol. 46(1), pp. 39-51.
[11] R. D. Middlebrook, Slobodan Cuk, “A General Unified Approach To Modeling Switching Converter Power Stages," IEEE Power Electronics Specialist Conference, Vol. 4, pp. 18-34, 1976.
[12] ADMC401 User's Guide/ Application Notes, Analog Devices, USA.
[13] Powersim Technologies, PSIM User's Guide, 2003, USA.

Sudhakarbabu. C was born in Ongole, A.P, India, in 1977. He received the B.E degree in Electrical and Electronics Engineering from C.R.R College of Engineering, Eluru, in 2000 and the M.Tech degree in Power Electronics from the National Institute of Technology Calicut, Kerala in 2002. From 2002 to 2003, he worked as a lecturer in V.R Siddhartha Engineering College, Vijayawada, India. Currently he is a research scholar in the Department of Electrical Engineering, Indian Institute of Technology Delhi, working towards his Ph.D. His main research interests include digital control of high frequency converters and their design.

Veerachary. M was born in Survail, India, in 1968. He received the Bachelor of Technology degree from the College of Engineering, JNT University, India, in 1992, the Master of Technology degree from the Regional Engineering College, India, in 1994, and the Dr.Eng Degree from the University of the Ryukyus, Okinawa, Japan, in 2002. Since July 2002, he has been with the Department of Electrical Engineering, Indian Institute of Technology Delhi, New Delhi, India, where he is currently an Assistant Professor. His fields of interest are power electronics and applications, modeling and simulation of large power electronic systems, design of power supplies for spacecraft systems, control theory application to power electronic systems, and intelligent controller applications to power supplies. Dr. Veerachary was the recipient of the IEEE Industrial Electronics Society Travel Grant Award for the year 2001, Best Paper Award at the International Conference on Electrical Engineering (ICEE-2000) held in Kitakyushu, Japan, and Best Researcher Award for the year 2002 from the President of the University of the Ryukyus, Japan. He is listed in Who’s Who in Science and Engineering’ 2003.